

01-04-00

A

01/03/00

jc715 U.S. PTO

UTILITY PATENT APPLICATION TRANSMITTAL
(Large Entity)*(Only for new nonprovisional applications under 37 CFR 1.53(b))*Docket No.
11675.130.1Total Pages in this Submission
28**TO THE ASSISTANT COMMISSIONER FOR PATENTS**

Box Patent Application

Washington, D.C. 20231

Transmitted herewith for filing under 35 U.S.C. 111(a) and 37 C.F.R. 1.53(b) is a new utility patent application for an invention entitled:

ANTIREFLECTIVE COATING LAYER

and invented by:

Yongjun Hu

jc617 U.S. PTO
09/476558

01/03/00

If a **CONTINUATION APPLICATION**, check appropriate box and supply the requisite information:☐ Continuation ☒ Divisional ☐ Continuation-in-part (CIP) of prior application No.: 08/918,690

Which is a:

☐ Continuation ☐ Divisional ☐ Continuation-in-part (CIP) of prior application No.:

Which is a:

☐ Continuation ☐ Divisional ☐ Continuation-in-part (CIP) of prior application No.:

Enclosed are:

Application Elements

1. ☒ Filing fee as calculated and transmitted as described below
2. ☒ Specification having 28 pages and including the following:
 - a. ☒ Descriptive Title of the Invention
 - b. ☒ Cross References to Related Applications *(if applicable)*
 - c. ☐ Statement Regarding Federally-sponsored Research/Development *(if applicable)*
 - d. ☐ Reference to Microfiche Appendix *(if applicable)*
 - e. ☒ Background of the Invention
 - f. ☒ Brief Summary of the Invention
 - g. ☒ Brief Description of the Drawings *(if drawings filed)*
 - h. ☒ Detailed Description
 - i. ☒ Claim(s) as Classified Below
 - j. ☒ Abstract of the Disclosure

UTILITY PATENT APPLICATION TRANSMITTAL
(Large Entity)

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Docket No.
11675.130.1

Total Pages in this Submission
28

Application Elements (Continued)

3. ☒ Drawing(s) *(when necessary as prescribed by 35 USC 113)*
- a. ☐ Formal Number of Sheets _____
- b. ☒ Informal Number of Sheets 4
4. ☒ Oath or Declaration
- a. ☐ Newly executed *(original or copy)* ☐ Unexecuted
- b. ☒ Copy from a prior application (37 CFR 1.63(d)) *(for continuation/divisional application only)*
- c. ☐ With Power of Attorney ☐ Without Power of Attorney
- d. ☐ DELETION OF INVENTOR(S)
Signed statement attached deleting inventor(s) named in the prior application,
see 37 C.F.R. 1.63(d)(2) and 1.33(b).
5. ☒ Incorporation By Reference *(usable if Box 4b is checked)*
The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under
Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby
incorporated by reference therein.
6. ☐ Computer Program in Microfiche *(Appendix)*
7. ☐ Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all must be included)*
- a. ☐ Paper Copy
- b. ☐ Computer Readable Copy *(identical to computer copy)*
- c. ☐ Statement Verifying Identical Paper and Computer Readable Copy

Accompanying Application Parts

8. ☒ Assignment Papers *(cover sheet & document(s))*
9. ☐ 37 CFR 3.73(B) Statement *(when there is an assignee)*
10. ☐ English Translation Document *(if applicable)*
11. ☒ Information Disclosure Statement/PTO-1449 ☐ Copies of IDS Citations
12. ☐ Preliminary Amendment
13. ☒ Acknowledgment postcard
14. ☒ Certificate of Mailing
- ☐ First Class ☒ Express Mail *(Specify Label No.):* EL 446 923 991 US

UTILITY PATENT APPLICATION TRANSMITTAL (Large Entity)

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Docket No.
11675.130.1

Total Pages in this Submission
28

Accompanying Application Parts (Continued)

15. ☐ Certified Copy of Priority Document(s) (if foreign priority is claimed)

16. ☒ Additional Enclosures (please identify below):

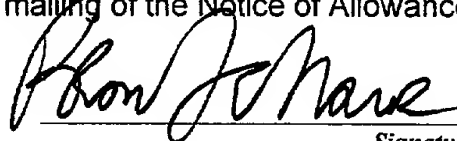
Associate Power of Attorney

Fee Calculation and Transmittal

CLAIMS AS FILED

For	#Filed	#Allowed	#Extra	Rate	Fee
Total Claims	40	- 20 =	20	x \$18.00	\$360.00
Indep. Claims	5	- 3 =	2	x \$78.00	\$156.00
Multiple Dependent Claims (check if applicable) <input type="checkbox"/>					\$0.00
BASIC FEE					\$690.00
OTHER FEE (specify purpose)					\$0.00
TOTAL FILING FEE					\$1,206.00

- ☒ A check in the amount of \$1,206.00 to cover the filing fee is enclosed.
- ☒ The Commissioner is hereby authorized to charge and credit Deposit Account No. 23-3178 as described below. A duplicate copy of this sheet is enclosed.
- ☐ Charge the amount of _____ as filing fee.
- ☒ Credit any overpayment.
- ☒ Charge any additional filing fees required under 37 C.F.R. 1.16 and 1.17.
- ☐ Charge the issue fee set in 37 C.F.R. 1.18 at the mailing of the Notice of Allowance, pursuant to 37 C.F.R. 1.311(b).



Signature

Bradley K. DeSandro, Reg. No. 34,521
WORKMAN, NYDEGGER & SEELEY
1000 Eagle Gate Tower
60 East South Temple
Salt Lake City, Utah 84111
Telephone: (801) 533-9800
Fax: (801) 328-1707

Dated: January 3RD, 2000

CC:

CERTIFICATE OF MAILING BY "EXPRESS MAIL" (37 CFR 1.10)

Applicant(s): Yongjun Hu

Docket No.

11675.130.1

Serial No.

Not yet assigned

Filing Date

Herewith

Examiner

Not yet assigned

Group Art Unit

Not yet assigned

Invention: ANTIREFLECTIVE COATING LAYER

jc617 U.S. PRO
09/476558

01/03/00

I hereby certify that this Patent Application and related documents

(Identify type of correspondence)

is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under

37 CFR 1.10 in an envelope addressed to: The Assistant Commissioner for Patents, Washington, D.C. 20231 on

January 3, 2000

(Date)

Peggy R. Huft

(Typed or Printed Name of Person Mailing Correspondence)

(Signature of Person Mailing Correspondence)

EL 446 923 991 US

("Express Mail" Mailing Label Number)

Note: Each paper must have its own certificate of mailing.

TRANSMITTAL LETTER
(General - Patent Pending)

Docket No.
11675.130.1

In Re Application Of: **Yongjun Hu**

Serial No.
Not yet assigned

Filing Date
Herewith

Examiner
Not yet assigned

Group Art Unit
Not yet assigned

Title: **ANTIREFLECTIVE COATING LAYER**

TO THE ASSISTANT COMMISSIONER FOR PATENTS:

Transmitted herewith is:

Transmittal of Utility Patent Application; Patent Application; Four (4) Sheets of Informal Drawings; Declaration & Oath; Assignment; Associate Power of Attorney; Information Disclosure Statement; PTO Form 1449; Check No. 113159 in the amount of \$1,206.00 ; Certificate of Express Mailing, No. EL 446 923 991 US; Postcard

In the above identified application.

- ☐ No additional fee is required.
- ☒ A check in the amount of **\$1,206.00** is attached.
- ☒ The Assistant Commissioner is hereby authorized to charge and credit Deposit Account No. **23-3178** as described below. A duplicate copy of this sheet is enclosed.
- ☐ Charge the amount of
- ☒ Credit any overpayment.
- ☒ Charge any additional fee required.


Signature

Dated: January 3rd, 2000

Bradley K. DeSandro, Reg. No. 34,521
WORKMAN, NYDEGGER & SEELEY
1000 Eagle Gate Tower
60 East South Temple
Salt Lake City, Utah 84111
Telephone: (801) 533-9800
Fax: (801) 328-1707

I certify that this document and fee is being deposited on _____ with the U.S. Postal Service as first class mail under 37 C.F.R. 1.8 and is addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231.

Signature of Person Mailing Correspondence

Typed or Printed Name of Person Mailing Correspondence

CC:

[illegible]

CORRESPONDENCE INFORMATION

APPLICATION INFORMATION

REPRESENTATIVE INFORMATION

CONTINUITY INFORMATION

```
Source:: PrintEFS Version 1.0.1
```

PATENT APPLICATION
Docket No. 11675.130.1

of

for

ANTIREFLECTIVE COATING LAYER

WORKMAN, NYDEGGER & SEELEY

A PROFESSIONAL CORPORATION

ATTORNEYS AT LAW

ATTORNEYS AT LAW
1000 EAGLE GATE TOWER

1000 LAQUELLE GAYLE TOWERS
60 EAST SOUTH TEMPLE

SALT LAKE CITY, UTAH 84111

1. Related Applications

This is a divisional application of US Patent Application Serial No. 08/918,690, filed on August 21, 1997, titled Antireflective Coating Layer and Method of Making which is incorporated herein by reference.

BACKGROUND OF THE INVENTION

2. The Field of the Invention

The present invention relates to the fabrication of integrated circuits. More particularly, the present invention relates to an anti-reflective enhancement for integrated circuit fabrication. In particular, the present invention relates to an anti-reflective enhancement for reducing critical dimension loss during mask patterning. More particularly, the present invention relates to formation of a metal silicon nitride antireflective coating layer that resist "foot poisoning" of a masking layer and its detrimental effects.

3. The Relevant Technology

In the microelectronics industry, a substrate refers to one or more semiconductor layers or structures which includes active or operable portions of semiconductor devices. In the context of this document, the term "semiconductive substrate" is defined to mean any construction comprising semiconductive material, including but not limited to bulk semiconductive material such as a semiconductive wafer, either alone or in assemblies comprising other materials thereon, and semiconductive material layers, either alone or in assemblies comprising other materials. The term substrate refers to any supporting structure including but not limited to the semiconductive substrates described above.

In the microelectronics industry, the process of miniaturization entails shrinking the size of individual semiconductor devices and crowding more semiconductor devices within a given unit area. With miniaturization, problems arise such as proper electrical isolation

between components. Attempts to isolate components from each other in the prior art are constrained by photolithographic limits of about 0.25 microns. One way to form structures that electrically isolate conductive materials on a semiconductor substrate from each other is to use photolithography in patterning dielectrics layers upon the semiconductor substrate.

To form a metallization wiring layer on a semiconductor substrate by photolithography, a photoresist mask is used to pattern the metallization wiring layer. The mask has directed therethrough a beam of light, such as ultraviolet (UV) light and deep UV (DUV) light (~250 nm), to transfer a pattern through an imaging lens from a photolithographic template to a photoresist coating which has been applied to the structural layer being patterned. The pattern of the photolithographic template includes opaque and transparent regions with selected shapes that match, respectively, openings and intact portions intended to be formed into the photoresist coating. The photolithographic template is conventionally designed by computer assisted drafting and is of a much larger size than the semiconductor substrate on which the photoresist coating is located. Light is directed through the photolithographic template and is focused on the photoresist coating in a manner that reduces the pattern of the photolithographic template to the size of the photolithographic coating and that develops the portions of the photoresist coating that are unmasked and are intended to remain. The undeveloped portions are thereafter removed. Other photolithographic techniques for formation of device features are also possible.

As dimensions shrink below about 0.25 microns, the prior art technique of forming metallization wiring layers becomes more difficult to achieve. Light that is reflected during exposure of a photoresist tends to blur the boundary between two metallization lines and the space therebetween. This blurring can cause wider metallization lines than designed, which excessive width will either bridge and short out the circuit or will cause unwanted "cross talk" such that the device is rendered defective.

1 In general, the blurred edge of a critically dimensioned photoresist layer caused by
2 reflected light in photolithographic techniques also result in problems in contact corridors,
3 vias, wiring trenches, and isolation trenches, where the dimensions are patterned below about
4 0.25 microns. For example, a contact corridor that is too wide will cause notching into a gate
5 stack during a contact corridor etch. Notching causes encroachment into conductive areas
6 of an adjacent gate stack and filling the contact corridor with metallization material can cause
7 a short to occur between the contact and the conductive elements of the adjacent gate stack.
8 A wiring trench that is too wide will cause "cross talk" with the wiring in a neighboring
9 trench so as so to compromise speed and accuracy of the integrated circuit associated
10 therewith.

11 The resolution with which a pattern can be transferred to the photoresist coating
12 from the photolithographic template is currently limited in commercial applications to widths
13 of about 0.25 microns. In turn, the dimensions of the openings and intact regions of the
14 photoresist mask, and consequently the dimensions of the shaped structures that are formed
15 with the use of the photoresist mask, are correspondingly limited. Photolithographic
16 resolution limits are thus a barrier to further miniaturization of integrated circuits.
17 Accordingly, a need exists for an improved method of forming semiconductor device
18 features that have a size that is reduced from what can be formed with conventional
19 photolithography.

20 During photolithography, reflected light that occurs during exposure of a mask tends
21 to blur the desired image because the reflected light escapes beyond exposed regions on the
22 photoresist. The blurring problem is caused by reflected light affecting areas of the
23 photoresist that are outside the design pattern.

24 Figure 1 illustrates the problem of blurring caused by reflected light that occurs
25 during exposure of a photoresist. A semiconductor structure 10 may be, for example, a
26 semiconductor substrate 12 that was designed to have a width D, but due to blurring caused

1 by reflectivity of patterning light from structures beneath the photoresist, semiconductor
2 substrate 12 has an actual width A. The variance between design width D and actual width
3 A is illustrated as the distance $2(B/2)$ or B. By way of example, semiconductor substrate 12
4 was designed to have a width D of 10 in arbitrary units, but due to blurring caused from
5 reflectivity, the actual width A is nine in arbitrary units. It can be seen that a ten percent
6 variance between design and actual width has occurred.

7 As miniaturization technology continues, a blurring variance of B as illustrated in
8 Figure 1 will increase relative to an ever-decreasing design width D. Thus, as also illustrated
9 in Figure 1, a miniaturized semiconductor substrate 12' that may have a design width D' of
10 two and one-half in arbitrary units but with the variance of B, will have the effect of causing
11 a 40 percent error. A variance of B may leave insufficient space upon miniaturized
12 semiconductor substrate 12' to form desired contacts or structures. It can be seen from the
13 demonstration illustrated in Figure 1 that the need to eliminate or substantially reduce
14 blurring must keep pace with miniaturization.

15 Another hindrance to photolithographic limitations are conventional antireflective
16 coating (ARC) schemes. Prior art methods for avoiding reflected light and its photoresist
17 blurring problems include using layers such as titanium nitride or organic materials that
18 reduce the reflected light in order to better control resolution of the photoresist. As the
19 ever-increasing pressure to miniaturize bears upon the microelectronics industry, the
20 conventional antireflective enhancements such as a titanium nitride layer, organic layers, or
21 other layers known in the art are proving inadequate at resolutions below about 0.25 microns.

22 One problem at a dimension below about 0.25 microns is that of fouling caused by
23 titanium nitride or organic materials. Fouling is defined as a tendency for a selected
24 antireflective layer to resist staying within preferred boundaries. Resistance to staying within
25 preferred boundaries tends to cause photolithographic techniques to be compromised.
26

When the ARC is a polymer film, it is applied directly to the semiconductor structure to a thickness of about 0.5 microns and photoresist is deposited on top of the ARC. The ARC then has the function of absorbing most of the radiation used during exposure of the photoresist that penetrates the photoresist material. Both standing wave effects and destructive scattering of light due to topographical features are suppressed with use of the ARC. A disadvantage of a polymer film ARC is that the process is increased in complexity and dimensional control may be lost. A polymer film ARC requires application by spin coating of the ARC material and pre-baking of same before applying the photoresist material. A problem of removing the ARC exists following an etch. For example, during anisotropic etching, portions of a photoresist are mobilized and form a liner within a recess that is being etched that further assists in achieving the anisotropic etch. Due to the anisotropic etch, however, the photoresist that was mobilized may have mingled with other elements that cause it to resist removal by conventional stripping techniques. This resistance to stripping requires stripping solutions that have a chemical intensity that may detrimentally effect the structure that was achieved during the anisotropic etch. As such, use of a substance that is intended to aid anti-reflectivity can result in the benefit thereof being mitigated by the requirement of a more chemically intensive stripping solution treatment.

Various attempts have been made to form antireflective coatings in order to further enhance miniaturization. One type of antireflective coating that has been developed includes metal nitrides, such as titanium nitride, and metal silicon nitrides. The prior art use of metal silicon nitrides and metal nitrides was developed for resolution limits at or above about 1.0 microns. At that resolution limit, there was little or no concern about the phenomenon called "foot poisoning" of the photoresist. Foot poisoning is the phenomenon of diffusion of a constituent of the antireflective layer out of the antireflective layer and into the photoresist material. Foot poisoning has the problem of changing the physical qualities of the photoresist material during processing so as to cause the photoresist material immediately

adjacent to the antireflective layer to spread or otherwise change. Figures 2-4 illustrate the phenomenon of foot poisoning as it develops during photoresist processing. In Figure 2 it can be seen that semiconductor structure 10 includes semiconductor substrate 12. Upon semiconductor substrate 12 there may be an insulation layer 14 such as borophosphosilicate glass (BPSG), or a silicate formed from tetraethylorthosilicate (TEOS) decomposition, or the like. Upon insulation layer 14 there is disposed a metallization layer 16 that is to be patterned into a system of superficial metallization lines. A prior art metal silicide or metal silicon nitride antireflective layer 18 is disposed upon metallization layer 16 and a masking layer 20 is disposed upon antireflective layer 18.

During processing of masking layer, as seen in Figure 3, a critical dimension D_C is formed by exposing masking layer 20 to form a patterned mask 22. During curing of patterned mask 22, nitrogen diffuses from antireflective layer 18 into patterned mask 22 and causes patterned mask 22 to expand at the interface between patterned mask 22 and antireflective layer 18. As seen in Figure 4, patterned mask 22 has formed a foot-poisoned mask 24 in which the critical dimension D_C has been lost and an actual dimension, D_A has resulted. When critical dimensions are in the range of about 0.5 to 1 microns, foot poisoning may not be a major concern. However, the trend of miniaturization has progressed to the point at which a resulting D_A in lieu of D_C is an undesirable variance. The need to reduce or eliminate foot poisoning can be appreciated as analogous to the need to reduce or eliminate blurring as illustrated in Figure 1. In other words, foot poisoning effects must be reduced in a manner that keeps pace with the process of miniaturization.

Another method of attempting to avoid reflected light is to use a metallic mask. Metallic materials, however, can cause contamination of the semiconductor structure beneath due to the high mobility of metal ions in wet chemical environments or in dry-etch vapors. Additionally, although a metallic mask may remain as part of a finished semiconductor

1 structure, a metallic mask may not be able to properly withstand high processing
2 temperatures sometimes required to achieve a preferred semiconductor structure.

3 What is needed is an antireflective coating scheme that does not substantially add
4 to fabrication cost and does not substantially reduce fabrication yield. What is also needed
5 is an antireflective coating scheme that imparts an antireflective quality to photolithographic
6 techniques not previously achieved in the prior art. What is also needed is an antireflective
7 coating scheme that does not cause fouling of the semiconductor structure. Additionally,
8 what is needed is an antireflective coating scheme that either does not require removal, or
9 that can be removed without causing contamination or damage to the semiconductor
10 structure. What is also needed is an antireflective coating scheme that facilitates a better
11 photoresist profile and better control of critical dimensions due to better prevention of
12 reflected light than is found in the prior art. What is also needed is an antireflective coating
13 scheme that, while resisting reflecting light, resists foot poisoning of the photoresist during
14 processing.
15
16
17
18
19
20
21
22
23
24
25
26

SUMMARY OF THE INVENTION

Antireflective structures according to the present invention comprise a metal silicon nitride composition in a layer that is superposed upon a layer to be patterned that would otherwise cause destructive reflectivity during photoresist patterning. The antireflective structure has the ability to absorb light used during photoresist patterning. The antireflective structure also has the ability to scatter unabsorbed light into patterns and intensities that are substantially ineffective to photoresist material exposed to the patterns and intensities.

Preferred antireflective structures of the present invention comprise a semiconductor substrate having thereon at least one layer of a silicon-containing metallic or silicon-containing metal nitride. The antireflective layer either absorbs reflected light or dissipates reflected light into patterns and intensities that do not substantially alter photoresist material that is exposed to the patterns and intensities. The semiconductor substrate will preferably have thereon a feature size with width dimension less than about 0.5 microns, and more preferably less than about 0.25 microns.

An antireflective structure according to the present invention comprises an antireflective layer that resists fouling of the semiconductor structure such as photoresist foot poisoning and that has the ability to absorb light or to scatter light into patterns and intensities that do not substantially effect photoresist material that is exposed by those patterns and intensities.

One preferred material for the inventive antireflective layer includes metal silicon nitrides. The metal silicon nitrides are of the general formula $M_xSi_yN_z$ wherein M is at least one transition metal, x is less than y, and z is in a range from about 0 to about 5y. Preferably, the Si will exceed M by about a factor of two. Addition of N is controlled by the ratio in the sputtering gas used in physical vapor deposition (PVD) to deposit the metal silicon nitride material, such as Ar/N.

Minimum reflectivity may be manipulated by adjusting the thickness of the antireflective layer. Minimum reflectivity may also be manipulated by nitrogen content in the inventive antireflective layer.

Tungsten is a preferred transition metal in the fabrication of the inventive antireflective coating. A preferred tungsten silicide target for the PVD process will have a composition of silicon between 1 and 4 in stoichiometric ratio to tungsten.

The inventive antireflective layer is amorphous or has a preferable grain size that is less than the film thickness of the antireflective layer. A grain size that is substantially the same or larger than the film thickness of the inventive antireflective layer will cause a substantially discontinuous film to form. A substantially discontinuous film will detrimentally allow for reflected light to escape from the metallization layer that is to be patterned.

Composite antireflective layers made of metal silicides or metal silicon nitrides may be fashioned according to the present invention depending upon a specific application.

Another type of composite antireflective layer may be made according to present invention in which antireflective layers made of metal silicides or metal silicon nitrides may be combined with rough or hemispherical grained polysilicon. In this embodiment, it may be advantageous to use the polysilicon as a later-used conductive layer such as the conductive material in a word line or as an etch stop structure.

The reflectivity exhibited by antireflective structures of the present invention can be described as the fraction of incident light energy that escapes from the surface of the antireflective structure when irradiated by photoresist patterning light under normal operating conditions.

In connection with preferred materials and preferred reflectivities of selected structures, it is also useful to describe the present invention in terms of a variance from the design geometry of an actual characteristic geometry of the structure being fabricated. It can

be appreciated that, as integrated circuit device geometries continue to shrink, the variance preferably either remains relatively constant or must also shrink.

The method of the present invention may be used to form various structures such as metallization layers. It is to be understood that the discussion of metallization layers is merely illustrative and not limiting of the inventive method. For example, isolation trenches, contact corridors, vias, stacked storage node wells, and wiring trenches are further non-limiting examples of structures that may also be formed by the inventive method and by use of the inventive antireflective structure.

BRIEF DESCRIPTION OF THE DRAWINGS

In order that the manner in which the above-recited and other advantages of the invention are obtained, a more particular description of the invention briefly described above will be rendered by reference to specific embodiments thereof which are illustrated in the appended drawings. Understanding that these drawings depict only typical embodiments of the invention and are not therefore to be considered to be limiting of its scope, the invention will be described and explained with additional specificity and detail through the use of the accompanying drawings in which:

Figure 1 is an elevational cross-section view of a semiconductor structure, illustrating the variance between a design dimension and an achieved dimension caused by the blurring effect of reflected light in the distortion of sub-micron critical dimensions in conventional photolithography.

Figure 2 is an elevation cross-section view of a semiconductor structure wherein an insulation layer is disposed upon a semiconductor substrate, a layer of metallization is disposed upon the insulation layer, an antireflective layer is disposed upon the layer of metallization, and a masking layer is disposed upon the antireflective layer.

Figure 3 is an elevation cross-section view of the semiconductor structure depicted in Figure 2, wherein the masking layer has been patterned to form a patterned mask with an ideal patterned critical dimension.

Figure 4 is an elevation cross-section view of the semiconductor structure in Figure 2, wherein the masking layer has been patterned to form a patterned mask, and wherein the phenomenon of foot poisoning is illustrated such that a critical dimension has been altered.

Figure 5 is a graph of the fraction of total reflectivity as a function of wavelength for a metal silicon nitride antireflective layer of a given chemical makeup for a series of varying thicknesses.

1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26

Figure 6 is a graph of the fraction of total reflectivity as a function of wavelength that illustrates the effect of measured reflectivity for antireflective layers that differ in nitrogen processing conditions during formation of the antireflective layer.

1
2
3
4
5
6
7
8
9
0
1
2
3
4
5
6
7
8
9
0
1
2
3
4
5
6

2
3
4
5
6
7
8

9

0
1
2
3
4

5
6
7
8
9
0
1
2
3
4
5
6

centimeters per minute (sccm). Thus, 30/20 represents 30 sccm Ar and 20 sccm N₂.

As it has been found that the presence of Si aids in resisting N₂ diffusion from the antireflective layer into the photoresist, a relationship is maintained that generally relates an increase of N₂ in the sputtering gas to an increase in Si in the net sputtering target. Thus, under similar sputtering conditions, the amount of N produced in an antireflective layer according to the present invention in a WSi₂ or a WSi_{2.55} target will preferably be less than the amount of N produced in an antireflective layer in a WSi_{2.7} target.

Figure 5 is an illustration of measured reflectivity of total incident light as a function of light wavelength. In Figure 5, five antireflective layers are depicted according to their specific measured reflectivities. The five antireflective layers have similar chemical compositions but have varying thicknesses. The curves in Figure 5 are labeled with reference numerals 85 through 200. Each reference numeral corresponds to a thickness of the inventive antireflective layer in Angstrom units (Å). The inventive antireflective layer was made by sputtering a titanium silicide target comprising a TiSi_{2.55} composition. Sputtering was carried out under the conditions of one kilowatt sputtering power, 400-700 volts sputtering potential, and a 30/20 Ar/N₂ sccm flow rate and ratio. The 200 Å thick antireflective layer was sputtered at 1 kW for ten seconds; the 160 Å thick antireflective layer was sputtered at 1 kW for eight seconds; the 120 Å thick antireflective layer was sputtered at 1 kW for six seconds; the 100 Å thick antireflective layer was sputtered at 1 kW for five seconds; and the 85 Å thick antireflective layer was sputtered at 0.8 kW and five seconds.

A simple linear regression of the observed approximate minimum reflectivities of the antireflective layers illustrated in Figure 5 demonstrates a substantially linear relationship between thickness of the inventive antireflective layer and minimum reflectivity. The 85 Å film has the minimum reflectivity right at the DUV wavelength (~ 250 nm).

Minimum reflectivity may also be manipulated by nitrogen content in the inventive antireflective layer. Figure 6 illustrates measured reflectivity of two inventive antireflective

1 layers, each having a thickness of about 120 Å, but having differing concentrations of
2 nitrogen therein. Each antireflective layer was fabricated under the conditions of 1 kW
3 sputtering power, six seconds sputtering time, and a $\text{WSi}_{2.55}$ tungsten silicide sputtering
4 target. The sputtering conditions variable was the nitrogen content in the sputtering gas as
5 illustrated by curves 30/30 and 30/20. It can be seen that sputtering with a higher nitrogen
6 ratio in the sputtering gas for a 120 Å thick antireflective layer fabricated will have a lower
7 minimum reflectivity than sputtering with a 30/20 Ar/N₂ ratio. It also has a lower
8 wavelength towards DUV at this minimum reflectivity.

9 Tungsten is a preferred transition metal in the fabrication of the inventive
10 antireflective coating. Tungsten is preferred because of its ability to form fine (*i.e.* less than
11 5 nm) grains of tungsten silicon nitride. Tungsten is also preferred because at a grain size
12 of 5 nm or smaller, tungsten grains are substantially amorphous.

13 A preferred tungsten silicide target will have a composition of silicon between 1 and
14 4 in stoichiometric ratio to tungsten. A more preferred tungsten silicide target will have a
15 composition of silicon between 2 and 4 in stoichiometric ratio to tungsten. Another preferred
16 target will have a silicon to tungsten ratio between 3 and 4. Commercially available tungsten
17 silicide targets may be used and sputtered at different voltage potentials in order to achieve
18 a preferred sputtering ratio of tungsten to silicon. For example, a low energy sputtering, *e.g.*
19 a sputtering at a potential between 400 and 700 volts at 1 kW, will tend to have a less
20 preferential sputtering between the tungsten and silicon components in the target. At higher
21 energy sputterings, preferential sputtering for tungsten over silicon may occur.

22 The inventive antireflective layer has a preferable grain size that is less than the film
23 thickness of the antireflective layer. A grain size that is substantially the same or larger than
24 the film thickness of the inventive antireflective layer will cause a substantially discontinuous
25 film to form. A substantially discontinuous film will allow for reflected light to escape
26 from, for example, the metallization layer 16 that is to be patterned.

1 It can now be appreciated that a grain size that is substantially 5 nm or less and/or
2 substantially amorphous such as including tungsten, fabricated under the conditions set forth
3 in the specification, can be found using other refractory or transition metals by reading the
4 specification and by routine experimentation.

5 Structures

6 Composite antireflective layers made of metal silicides or metal silicon nitrides may
7 be fashioned according to the present invention depending upon a specific application. In
8 many applications, it is presupposed that a metallization layer such as metallization layer 16
9 is being overlayed with the inventive antireflective layer.

10 Another type of composite antireflective layer may be made according to present
11 invention in which antireflective layers made of metal silicides or metal silicon nitrides may
12 be combined with rough or hemispherical grained polysilicon. In this embodiment, it may
13 be advantageous to use polysilicon as a later-used conductive layer such as the conductive
14 material in a word line or as an etch stop structure.

15 Reflectivity

16 The reflectivity exhibited by antireflective structures of the present invention can be
17 described as the fraction of incident light energy that escapes from the surface of the
18 antireflective structure when irradiated by photoresist patterning light under normal operating
19 conditions. Various ways of describing reflectivity may be expressed. For example, a simple
20 fraction of incident light energy may be given for a preferred reflectivity as illustrated in
21 Figures 5 and 6. A preferred reflectivity for the present invention is in a range from about
22 0 to about 30 percent, more preferably from about 5 to about 20 percent, and most preferably
23 from about 10 to about 15 percent.

24 Figure 5 illustrates the reflectivity of metal silicon nitride antireflective layers as a
25 function of incident light wavelength. Standard conditions for the antireflective layers
26 include fabrication thereof from a $WSi_{2.55}$ target with a sputtering gas flow ratio of Ar/N of

1 30/20. In each case, sputtering was carried out under 1 kW power conditions, and sputtering
2 times were varied in order to achieve a selected range of thicknesses. It can be seen from the
3 reflectivity curves in Figure 5 that minimal reflectivity for antireflective layers made of metal
4 silicon nitride material is a function of layer thickness for the layer thickness tested. Linear
5 regression of approximate minimal reflectivity as a function of layer thickness reveals a
6 substantially linear relationship therebetween. It can also be seen that the minimal
7 reflectivity of the inventive metal silicon nitride antireflective layers is in the DUV
8 wavelength range of below about 400 nm.

9 A second set of antireflective layers was made to discover the effect of nitrogen
10 content therein upon reflectivity. Figure 6 illustrates two antireflective layers of metal silicon
11 nitrides that were made from a $\text{WSi}_{2.55}$ target with sputtering gas flow ratios of Ar/N of 30/20
12 and 30/30. As it can be observed, the antireflective layer that was sputtered from a $\text{WSi}_{2.55}$
13 target with a sputtering gas flow ratio of Ar/N of 30/20 has a lower overall reflectivity than
14 the antireflective layer that was sputtered from a $\text{WSi}_{2.55}$ target with a sputtering gas flow
15 ratio of Ar/N 30/30. The same trend can also be used with increasing silicon content in a
16 tungsten silicide target.

17 By understanding the relationships illustrated in Figures 5 and 6, materials may be
18 selected by using such relationships as, for example, the Beer-Lambert law:

$$19 \quad I = I_0 \exp(-\epsilon \rho d) \quad (1),$$

20 where I is the reflected light intensity, I_0 is the initial light intensity, ϵ is the black-body
21 degree of opacity or light extinction coefficient of the material, ρ is the density of the
22 material, and d is the measured distance from the surface of the antireflective structure to a
23 detector.

24 It can be appreciated that various metal silicon nitride combinations can be selected
25 and tested that can be compared with the antireflective layers taught herein. It can be further
26 appreciated that one of ordinary skill in the art will be able to select from fouling-resistant,

1 light-dissipating, and light-absorbing combinations, and that a relationship between ρ and
2 ϵ can be used to choose equivalent materials to those that are disclosed herein.

3 Blurring Effects

4 In connection with preferred materials and preferred reflectivities of selected
5 structures, it is also useful to describe the present invention in terms of a variance from the
6 design geometry of an actual characteristic geometry of the structure being fabricated. A
7 mask may be designed with a first preferred characteristic geometry and, as illustrated in
8 Figure 1, the actual geometry exposed in photolithography will vary from the design
9 geometry. With geometries contemplated by the present invention, a variance of less than
10 10 percent is preferred and a variation of less than 5 percent is most preferred. It can be
11 appreciated that, as integrated circuit device geometries continue to shrink, the variance
12 preferably either remains relatively constant or must also shrink.

13 Applications

14 The method of the present invention may be used to form various structures with
15 preferred geometries such as metallization layers. It is to be understood that the discussion
16 of metallization layers is merely illustrative and not limiting of the inventive method. For
17 example, isolation trenches, contact corridors, vias, stacked storage node wells, and wiring
18 trenches are further non-limiting examples of structures that may also be formed by the
19 inventive method and by use of the inventive antireflective structure.

20 Preferred geometries of the present invention are geometries below 0.25 microns.
21 More preferred geometries achieved by using the inventive antireflective layer are geometries
22 below about 0.22 microns. Even more preferred geometries are below 0.2 microns. Highly
23 preferred geometries are achieved below 0.1 microns, and the present invention may be used
24 to achieve patterning geometries of about 0.07 microns.

25 The present invention may be embodied in other specific forms without departing
26 from its spirit or essential characteristics. The described embodiments are to be considered

1 in all respects only as illustrated and not restrictive. The scope of the invention is, therefore,
2 indicated by the appended claims and their combination in whole or in part rather than by the
3 foregoing description. All changes that come within the meaning and range of equivalency
4 of the claims are to be embraced within their scope.

5 What is claimed and desired to be secured by United States Letters Patent is:
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26

1. An ARC comprising:
a material substantially composed of $M_xSi_yN_z$, wherein:
M is at least one transition metal;
y is greater than x; and
z is in a range from about 0 to about 5y.
2. An ARC as defined in Claim 1, wherein M includes at least two transition metals of the configuration $M1_rM2_{1-r}$, wherein r is in a range from 0 to 1.
3. An ARC as defined in Claim 2, wherein M1 is tungsten and r is 1.
4. An ARC as defined in Claim 2, wherein M1 is tungsten, M2 is titanium, and r is about 0.5.
5. An ARC as defined in Claim 1, wherein M is tungsten, x is 1, and Si is in a range from about 1.5 to about 5.
6. An ARC as defined in Claim 1, wherein said ARC has a thickness range from about 25 Angstroms to about 1,000 Angstroms.
7. An ARC as defined in Claim 1, wherein said ARC has a thickness range from about 50 Angstroms to about 400 Angstroms.
8. An ARC as defined in Claim 1, wherein said ARC has a thickness range from about 85 Angstroms to about 200 Angstroms.

- 1 9. An ARC as defined in Claim 1, wherein y equals about 2x.
- 2
- 3 10. An ARC as defined in Claim 1, wherein y equals about 2.55x.
- 4
- 5 11. An ARC as defined in Claim 1, wherein y equals about 2.7x.
- 6
- 7 12. An ARC as defined in Claim 1, wherein M includes a combination of
- 8 M₁M₂_{1-r}, wherein r is in the range from 0 to 1, and wherein M1 and M2 are selected from
- 9 the group consisting of Sc, Ti, Zr, Nb, Ta, Mo, W, Co, and Ni and wherein M1 is not M2.
- 10
- 11 13. An ARC as defined in Claim 1, wherein z is in a range from about 1y to about
- 12 2y.
- 13
- 14 14. An ARC as defined in Claim 1, further composed of hemispherical grained
- 15 polysilicon.
- 16
- 17 15. An ARC as defined in Claim 1, wherein the material substantially composed
- 18 of M_xSi_yN_z is a metal silicon nitride ternary compound.
- 19
- 20 16. A semiconductor structure comprising:
- 21 a semiconductor substrate;
- 22 an ARC over the semiconductor substrate, said ARC being composed of a
- 23 metal silicon nitride ternary compound, wherein the metal is at least one metal
- 24 selected from the group consisting of Sc, Ti, Zr, Nb, Ta, Mo, W, Co, Al, and Ni.
- 25
- 26

17. The semiconductor structure as defined in Claim 16, wherein the metal silicon nitride ternary compound is selected from the group consisting of titanium tungsten nitride, tungsten aluminum nitride, and titanium aluminum nitride

18. The semiconductor structure as defined in Claim 16, wherein said ARC has a thickness range from about 25 Angstroms to about 1,000 Angstroms.

19. The semiconductor structure as defined in Claim 16, wherein the metal is selected from the group consisting of $\text{Ti}_r\text{W}_{1-r}$, $\text{W}_r\text{Al}_{1-r}$, or $\text{Ti}_r\text{Al}_{1-r}$.

20. The semiconductor structure as defined in Claim 16, wherein:
said ARC has a film thickness and a grain size; and
the grain size of the ARC is less than the film thickness or is amorphous.

21. The semiconductor structure as defined in Claim 16, wherein the metal silicon nitride ternary compound is $M_xSi_yN_z$, M is a metal, x is greater than zero, y is greater than 2x, and z is in a range from about 1y to about 5y.

22. The semiconductor structure as defined in Claim 21, wherein z is in a range from about $1y$ to about $2y$.

23. The semiconductor structure as defined in Claim 21, wherein said ARC is further composed of hemispherical grained polysilicon.

24. The semiconductor structure as defined in Claim 16, wherein the ARC reflects incident light energy in a reflectivity that is in a range from 0 percent to about 30 percent.

1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26

25. The semiconductor structure as defined in Claim 16, wherein:
the ARC is upon a formation that is selected from the group consisting of an
isolation trench, a contact corridor, a via, a stacked storage node well, and a wiring
trench.

26. A semiconductor structure comprising:
a semiconductor substrate;
an ARC upon said semiconductor substrate, said ARC being composed of a
metal silicon nitride ternary compound $M_xSi_yN_z$, wherein:

x is greater than zero;

y is greater than x;

z is greater than zero and less than about 5y;

M is at least two transition metals composed of $M1_rM2_{1-r}$;

r is in a range from 0 to 1;

M1 and M2 are selected from the group consisting of Sc, Ti, Zr, Nb,
Ta, Mo, W, Co, and Ni; and

M1 is not M2.

27. The semiconductor structure as defined in Claim 26, wherein said ARC has
a thickness range from about 25 Angstroms to about 1,000 Angstroms.

28. The semiconductor structure as defined in Claim 26, wherein said ARC is also
composed of hemispherical grained polysilicon.

1 29. A semiconductor structure comprising:
2 an electrically insulative layer upon a semiconductor substrate;
3 a patterned electrically conductive metal line upon electrically insulative
4 layer;
5 an ARC upon said electrically conductive metal line, said ARC being
6 composed of a metal silicon nitride ternary compound $M_xSi_yN_z$, wherein:

7 x is greater than zero,

8 M is at least one transition metal selected from the group consisting
9 of Sc, Ti, Zr, Nb, Ta, Mo, W, Co, Al, and Ni;

10 y is greater than x; and

11 z is greater than about 0 and less than about 5y.

12
13 30. The semiconductor structure as defined in Claim 29, wherein said ARC has
14 a thickness range from about 25 Angstroms to about 1,000 Angstroms.

15
16 31. The semiconductor structure as defined in Claim 29, wherein said ARC is also
17 composed of hemispherical grained polysilicon.

18
19 32. A semiconductor structure comprising:
20 a semiconductor substrate;
21 an ARC over the semiconductor substrate, said ARC being composed of a
22 metal silicide binary compound, wherein the metal is at least one metal selected
23 from the group consisting of Sc, Ti, Zr, Nb, Ta, Mo, W, Co, Al, and Ni.

- 1 33. The semiconductor structure as defined in Claim 32, wherein:
2 the metal silicide binary compound is $M1_rM2_{1-r}Si_s$;
3 M1 and M2 are both said at least one metal and are selected from said group;
4 M1 is not M2;
5 r is in a range from 0 to 1; and
6 s is greater than zero.
7
- 8 34. The semiconductor structure as defined in Claim 33, wherein M1 and M2 are
9 selected from the group consisting of Sc, Ti, Zr, Nb, Ta, Mo, W, Co, and Ni.
10
- 11 35. The semiconductor structure as defined in Claim 33, wherein M1 and M2 are
12 selected from the group consisting of Sc, Ti, Nb, Ta, W, Co, and Ni.
13
- 14 36. The semiconductor structure as defined in Claim 32, wherein:
15 the metal silicide binary compound is M_xSi_y ;
16 M is tungsten, x is 1, and Si is in a range from about 1.5 to about 5.
17
- 18 37. The semiconductor structure as defined in Claim 32, wherein said ARC is
19 further composed of hemispherical grained polysilicon.
20
- 21 38. The semiconductor structure as defined in Claim 32, wherein:
22 said ARC has a film thickness and a grain size; and
23 the grain size of the ARC is less than the film thickness or is amorphous.
24
- 25 39. The semiconductor structure as defined in Claim 32, wherein the ARC reflects
26 incident light energy in a reflectivity that is in a range from 0 percent to about 30 percent.

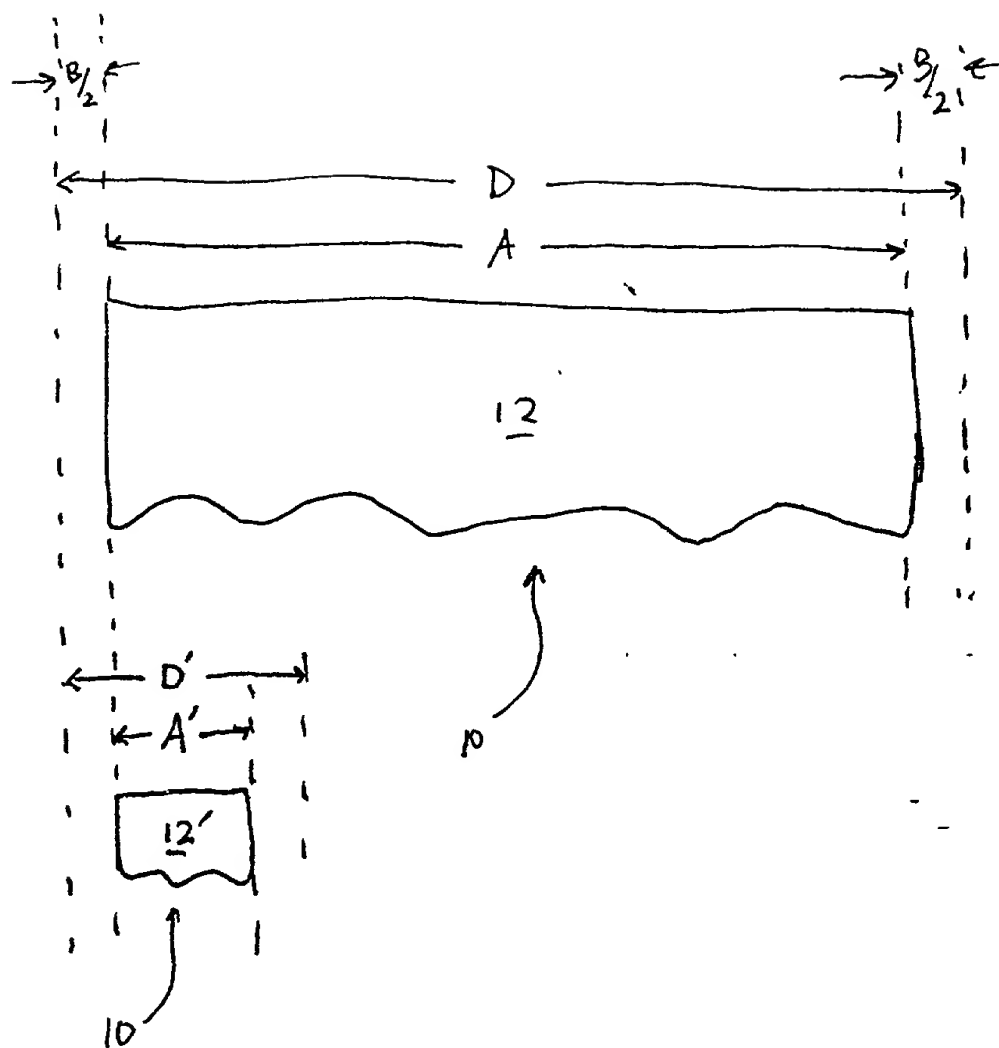
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26

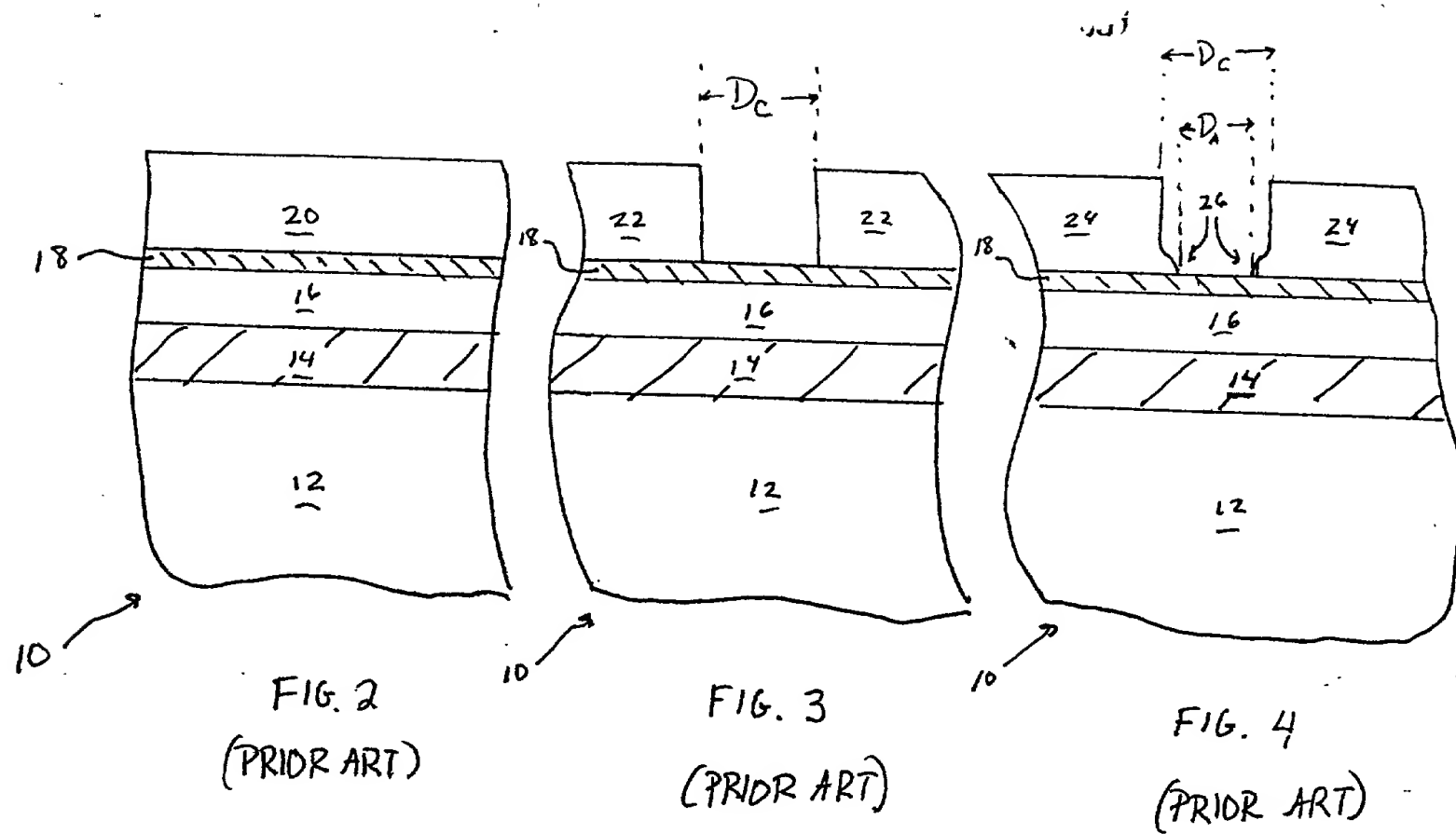
40. The semiconductor structure as defined in Claim 32, wherein:
the ARC is upon a formation that is selected from the group consisting of an
isolation trench, a contact corridor, a via, a stacked storage node well, and a wiring
trench.

- 1
- 2
- 3
- 4
- 5
- 6
- 7
- 8
- 9
- 10
- 11
- 12
- 13
- 14
- 15
- 16
- 17
- 18
- 19
- 20
- 21
- 22
- 23
- 24
- 25
- 26

G\DATA\PAT\11675130 1PA

FIG. 1





2025 RELEASE UNDER E.O. 14176

DECLARATION, POWER OF ATTORNEY, AND PETITION

I, Yongjun Hu, declare: that I am a citizen of the People's Republic of China; that my residence and post office address is 2470 Canal Street #203, Boise, Idaho 83705; that I verily believe I am the original, first, and sole inventor of the subject matter of the invention or discovery entitled ANTIREFLECTIVE COATING LAYER AND METHOD OF MAKING, for which a patent is sought and which is described and claimed in the specification attached hereto; that I have reviewed and understand the contents of the above-identified specification, including the claims; and that I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Section 1.56(a) of Title 37 of the Code of Federal Regulations.

I declare further that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful, false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful, false statements may jeopardize the validity of the application or any patent issuing thereon.

I hereby appoint as my attorneys and/or patent agents: H. ROSS WORKMAN, Registration No. 25,230; RICK D. NYDEGGER, Registration No. 28,651; DAVID O. SEELEY, Registration No. 30,148; JONATHAN W. RICHARDS, Registration No. 29,843; JOHN C. STRINGHAM, Registration No. P-40,831; MICHAEL F. KRIEGER, Registration No. 35,232; BRADLEY K. DeSANDRO, Registration No. 34,521; JOHN M. GUYNN, Registration No. 36,153; GREGORY M. TAYLOR, Registration No. 34,263; DANA L. TANGREN, Registration No. 37,246; ERIC L.

MASCHOFF, Registration No. 36,596; KEVIN B. LAURENCE, Registration No. 38,219; SUSAN K. MORRIS, Registration No. 39,780, JEFFREY L. RANCK, Registration No. 38,590; C. J. VEVERKA, Registration No. P-40,858; JONATHAN D. WOOD, Registration No. 39,076; ROBYN L. PHILLIPS, Registration No. 39,330; DAVID B. DELLENBACH, Registration No. 39,166; TIMOTHY M. FARRELL, Registration No. 37,321; LENA I. VINITSKAYA, Registration No. 39,448; JOHN N. GREAVES, Registration No. 40,362, KEVIN K. JOHANSON, Registration No. 38,506; MICHAEL L. LYNCH, Registration No. 30,871; and LIA P. DENNISON, Registration No. 34,095, with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith. All correspondence and telephonic communications should be directed to:

BRADLEY K. DeSANDRO
WORKMAN, NYDEGGER & SEELEY
1000 Eagle Gate Tower
60 East South Temple
Salt Lake City, Utah 84111

Wherefore, I pray that Letters Patent be granted to me for the invention or discovery described and claimed in the foregoing specification and claims, declaration, power of attorney, and this petition.

Signed at Boise, Idaho, this 20 day of

August, 1997.

Inventor: 

Yongjun Hu
2470 Canal Street #203
Boise, Idaho 83705

G:\DATA\WPDOCS\DF\MICRON\11675130.DEC
Rev. 12/96

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of)
)
	Yongjun Hu)
)
Serial No.:	Not Yet Assigned)
)
Filed:	January 3, 2000)
)
For:	ANTIREFLECTIVE COATING LAYER)
)
Examiner:	Not Yet Assigned)

ASSOCIATE POWER OF ATTORNEY

The Assistant Commissioner of Patents
and Trademarks
Washington, D. C. 20231

Sir:

Please recognize the following attorneys: RICHARD C. GILMORE, Registration No. 37,335; CHARLES L. ROBERTS, Registration No. 32,434; JESUS JUANOS i TIMONEDA, Registration No. 43,332; DAVID R. TODD, Registration No. 41,348; STEPHEN D. PRODNUK, Registration No. 43,020; PARRISH R. FREEMAN, Jr., Registration No. 42,556; R. BURNS ISRAELSEN, Registration No. 42,685; ADRIAN J. LEE, Registration No. 42,785; and KYLE H. FLINDT, Registration No. 42,539, as associate attorneys for me in the above-entitled application.

Please address all future written and telephonic communications to:

Bradley K. DeSandro
WORKMAN, NYDEGGER & SEELEY
1000 Eagle Gate Tower
60 East South Temple
Salt Lake City, Utah 84111

Dated this 3rd day of January 2000.

Respectfully submitted,



BRADLEY K. DeSANDRO
Attorney for Applicant
Registration No. 34,521

WORKMAN, NYDEGGER & SEELEY
1000 Eagle Gate Tower
60 East South Temple
Salt Lake City, Utah 84111
Telephone: (801) 533-9800
Facsimile: (801) 328-1707